

ABSTRACT

A synchronized sampled data system comprising two or more sampled data circuits (10) each sharing a common databus (12) providing instructional words. Each sampled data system has an output (20) synchronized and phase shifted with respect to the other by preloading a 5 unique start word into its respective internal counter (22) via a common control line. After initialization, each counter is clocked in synchronization with the other by a common clock (SCLK), such that the counter's counts remain the predetermined count difference from the other, and respective circuit output (20) maintains the corresponding phase relationship. The present invention finds particular advantages controlling switching power supplies and A to D converters. A desired phase lag can be established with a granularity of 1/M clock cycles. The present invention achieves lower input ripple current, lower in-band conducted emissions and better signal to noise ratio of the whole system.

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